WHAT IS CLAIMED IS:

1. A method of forming damascene pattern in a semiconductor device, the method comprising:

forming an insulating layer on a bottom wiring;

forming via holes exposing a part of the bottom wiring by removing the insulating layer selectively;

filling insides of the via holes to a prescribed thickness using non-conductive material;

forming an anti-reflection layer on the via holes and the insulating layer;

forming a mask pattern for trench etching in the insulating layer on which the anti-reflection layer is formed; and

forming a damascene pattern after forming trenches using the mask pattern.

2. The method of claim 1, wherein the filling comprises:

forming a non-conductive material layer on the insulating layer in which the via holes are formed; and

removing the non-conductive material layer selectively to make the insulating layer become exposed and to make the non-conductive material remain for a prescribed thickness.

3. The method of claim 2, wherein the non-conductive material layer is made of photoresist.

4. The method of claim 2, wherein said selective removal utilizes entire surface dry etching process or chemical mechanical polishing process.